Applicants:	Walter Fix et al.
Serial No.:	10/562,869
Filed:	April 7, 2006
For:	Logic Gate with a Potential-Free Gate Electrode for Organic Integrated Circuits
Examiner:	Eva Y. Montalvo Art Unit: 2814
Attorney Dkt:	411000-144 Customer No. 27162

REPLY BRIEF

MS Appeal Brief
Commissioner for Patents
Box 1450
Alexandria, VA 22313-1450

Sir:

This paper is in reply to the Examiner's answer in response to applicants' brief raising new issues not in the final Office Action rejection nor otherwise of record as being proffered in writing by the Office with particularity and the required evidence. Such relevant evidence is missing. The answer states, page 6, first full paragraph, as to applicants' disclosure as quoted, "This teaching does not exclude the gate electrode of the charging FET from being coupled to other elements in the circuit, to 'thereby provide a potential at the gate electrode of the charging FET.' "

This statement is directed to irrelevant subject matter as to what the applicants' application discloses as to the new matter issue. Whether or not applicants' disclosure supports the claim in issue is not relevant to whether or not one of skill would want to modify the disclosure for some unknown or different purpose than that of the disclosed invention. This conclusion has nothing to do with what is disclosed.

The issue is: does or does not the specification and drawings support the claimed subject matter in question that is alleged to have no support in the application?

The Answer's statement above does not address the reasoned facts supplied in applicants' brief as to the specification passages and drawing figure thereof that applicants urge as providing the necessary support for the claim terminology in issue. What others might do with the disclosed structures is not relevant.

The Answer, more importantly raises a new issue for the first time, not previously of record in the final Action or any other Action provided by the PTO. Applicants were never previously provided such an issue by the PTO in writing in any of its prior Office Actions. This issue is raised in writing for the first time in response to applicants' appeal brief.

This issue raised by the Answer is that

> "all capacitors have imperfections within the capacitor material that create parasitic resistance (equivalent series resistance) (ESR),"

attaching various pages of Wikipedia definitions concerned with ESR (3 pages) and a definition of a capacitor (16 pages) such that the claimed subject matter as to the capacitor solely providing a potential at the gate electrode is not disclosed by applicants. This conclusion is hypertechnical and in error.

The evidence supplied by the answer does not support the conclusion that all capacitors have ESR or an ESR that is sufficiently significant as to affect operation of the relevant circuit as discussed in more detail below wherein the so called ESR potential is so small or trivial that it is negligible for all practical purposes of the circuit. The supplied evidence expressly states that not all capacitors have such ESR, or that some have ESR that is so small as to be negligible, or not in existence, mentioning for

example electrolytic capacitors that may exhibit such ESR and non-electrolytic capacitors that may exhibit no ESR. This is discussed in more detail below.

Applicants' representative figure 4 shows the so called capacitor involved to which the claimed subject matter is directed as comprising thin layers of deposited material forming an FET device. This, as would be understood by one of ordinary skill, is not an electrolytic capacitor. Therefore, according to the Examiner's evidence, such a capacitor would not normally exhibit ESR as discussed below. No evidence is supplied that discloses an FET as disclosed that must always exhibit ESR. Such is only a mere possibility or probability. No authority is cited that supports the rejection of a new matter issue on the basis of possibilities and probabilities that might contradict the express disclosure of an applicant.

The specification clearly and expressly states ([0008]) of the published application

> "the organic logic gate according to the invention is characterized in that the gate electrode of the charging FET is potential-free."

It also states [0012]:

> "In the case of a capacitive coupling between gate electrode and source or drain electrode of a charging FET, it is possible to dispense with a direct electrical coupling between gate electrode and source or drain electrodes."

This statement expressly states there is no direct coupling between the gate electrode and a source or drain electrode of the charging FET. One of ordinary skill would interpret these statements as meaning there is no potential at the gate electrode created by a direct coupling, but only by the capacitive coupling. However, ESR, equivalent series resistance, by definition is a series resistance, as disclosed by the

cited evidence, is such a direct coupling as exhibited by lead resistance, or inherent resistances in a dielectric material that might be present or otherwise.

Therefore, one of ordinary skill would plainly understand that "the potential free" example at the gate electrode as expressed in [0008] is meant to refer to solely the capacitive coupling with no other direct coupling such as ESR that might create a potential at the gate outside the pure capacitance provided as provided by the statement in [0012]. One of ordinary skill is not without common sense.

That is, if there is ESR, if any, it would be so small as to be negligible and disregarded in the disclosed embodiment in which there is expressly no direct coupling between the involved electrodes to create such a potential (which would thus exclude ESR as well). Thus, the specification contemplates an embodiment when an ideal or real world capacitor is coupled between the involved electrodes such that a potential that is provided at the gate electrode is solely that due to the capacitive coupling, and not be any direct coupling, e.g., resistive of any nature, whether by parasitic elements or discrete elements.

In view of this express disclosure, applicants are perplexed as to the conclusion that the specification does not support the claimed subject matter

All patents are directed to ideal components, not imperfect devices that may or may not exhibit a parameter effective to alter the operation of the claimed device. Trivial imperfections in real world devices, that may or may not be effective relative to the claim or operation of the disclosed device, without further evidence, are improper to support a rejection. This is especially so in view of applicants' express disclosure of an

embodiment wherein there is no direct coupling to provide a potential free gate electrode outside the capacitive coupling.

This issue, raised for the first time now during this appeal, has nothing to do with a typical applicant's disclosure regarding electrical circuits having disclosed ideal (or real world) capacitors or other electronic components. The PTO has granted tens of thousands of patents directed to electrical and electronic circuits all related to such components, not to components that might have imperfections in the real world. Patents are not directed to such ancillary issues.

To the undersigned's knowledge, in over 40 years of preparing and prosecuting patent applications including untold numerous electronic circuits that include all sorts of electronic components, which can be cited if the Board desires, none involve an issue regarding parasitic resistances or inductances or other imperfections in ideal device as disclosed in such patents to the undersigned's knowledge. As far as the undersigned is concerned, all granted patents deal with ideal (or equivalent real world) components as a matter of general principal. None deal with so called inherent imperfections that might or might not result in so called ESR and so on.

Real world capacitors are widely available, widely distributed and purchased by those of ordinary skill. Such persons normally are skilled engineers or circuit designers familiar with detailed component specifications supplied by the component manufacturer. If significant ESR or related parameters are present in such components, the detailed manufacturer's specifications should or would include such information so the engineers or purchasers can deal with such issues and make a determination of

whether or not such parameters need to be dealt with individually upon purchase of such components.

In the real world, electrical components are purchased for their everyday technical descriptions, e.g., capacitor, inductor, resistor etc. Parasitic elements are not relevant to the name of such components as to what they are called when purchased and used in a circuit. In other words, a capacitor is just that, a capacitor, and is purchased by the ordinary purchaser under that description and used in this way. Thus if a circuit has two elements coupled solely by the capacitor, then it is axiomatic that a potential created at one element due to the presence of the capacitor is present due solely to that capacitive coupling, this is regardless of the inherent internal imperfections of the component. To reject this concept on the basis that the internal coupling is not capacitive, but resistive, is hypertechnical and contrary to the common understanding of such a component by one of ordinary skill. Such an interpretation should not be condoned in claim construction such that applicants' intent is distorted by unreasonable claim construction and their application rejected on such a hypertechnical construction of terms.

The claim in issue is directed to providing a potential at the gate electrode of the charging FET solely by the capacitive coupling between the gate electrode and one of the source/drain electrodes of the charging FET. If that capacitive coupling results in ESR, that potential is still provided by the capacitive coupling of a capacitor, and not by another external direct coupling as contemplated by the disclosure. Therefore, in this context, the term "capacitive coupling" means solely by the capacitor regardless if in fact such coupling introduces ESR. If the capacitor exhibits ESR, it still forms a capacitive

coupling and infringement would be determined on whether or not there is solely a capacitor between the involved electrodes or other circuit elements. The claim is plainly directed to a common everyday capacitor coupled between the involved electrodes and not based on its internal characteristics, whatever they may be. Whatever parasitic or other imperfect element is present in a capacitor is not considered as to calling and referring to a capacitor as such, it still is a capacitor, and when coupled between two electrodes, the electrodes are solely capacitive coupled as would be understood by one of ordinary skill.

Attached to the Answer is a copy of a Wikipedia description of ESR. As noted therein at page 1, in the Overview section, fourth paragraph:

> "Capacitors, inductors, and resistors are usually designed to minimise [sic] other parameters. In many cases this can be done to a sufficient extent that *parsitic* capacitance and inductance of a resistor, for example, <u>are so small as not to effect circuit operation</u>." (underlining added)

In other words, electronic components are well known by those of ordinary skill to be designed and constructed to minimize or eliminate and make ineffective such imperfections. At page 2, under the heading "CAPACITORS," first paragraph, the Wikipedia article states that

> "ESR of non-electrolytic capacitors tends to be fairly stable over time; for most purposes <u>real non-electrolytic capacitors can be treated as ideal components</u>." (underlining added)

An electrolytic capacitor is defined as:

> A capacitor consisting of two electrodes separated by an electrolyte; a dielectric film, usually a thin layer of gas, is formed on the surface of one electrode. Also known as electrolytic condenser.

McGraw Hill Dictionary of Scientific and Technical Terms, page 474, 1974.

Such electrolytic capacitors are not disclosed in applicants' application. What are disclosed are non-electrolytic capacitors comprising layers of printed or otherwise applied organic materials. Such materials do not comprise an electrolyte as disclosed by applicants.

Page 6, lines 3-5, of applicants' specification states:

> The capacitance 14 may be implemented for example by the gate electrode overlapping the source or drain electrodes.

Such does not form an electrolytic capacitor and no evidence of such is provided by the Answer to the contrary.

Page 6, lines 14-16, of applicants' specification states:

> The capacitance 16 may be implemented for example by the gate electrode overlapping the source or drain electrodes.

Such overlapping layers has not been shown by any convincing evidence that they must form an electrolytic capacitor and/or that significant circuit controlling effective values of ESR are present such that a potential is provided at the gate outside of the capacitive coupling, and no evidence of such is provided by the Answer. In respect of Fig. 4, the specification states at page 7, lines 9-11:

> The region 16 essentially defines the region of the capacitive coupling between the gate electrode 20 and the electrode 8.

In Fig. 4, it is plain that the two electrodes 8 and 12 are connected by a semiconductor layer 24. An insulator layer 26 is above the semiconductor layer 24. The gate electrode 20 is above the insulator layer. This disclosure relates to organic integrated circuits which are well known to comprise various layers of organic materials forming the

components as deposited layers by printing, vapor deposition, doctor blades, and similar process that deposit the organic layers one over the other. The capacitors formed by such components are not electrolytic and have no electrolytes, and no evidence is supplied by the Answer that such capacitors constructed as disclosed in fact exhibit parasitic ESR. However, even if such ESR were present, this still does not negate the fact that the electrodes involved are solely capacitively coupled so that a potential at the gate is provided solely by such capacitive coupling as would be provided solely by a capacitor component and none other.

As stated by the cited reference to Wikipedia, "for most purposes real non-electrolytic capacitors can be treated as ideal components." Such ideal components do not have parasitic elements. That is, the value of the so called parasitic elements are so small as to be negligible and of no concern on the operation of the circuit. Therefore, for these reasons, applicants' specification discloses the use of ideal or real world components exhibiting no such imperfections or effective imperfections as asserted by the Answer such that applicants have no support for the claimed subject matter.

In the alternative, applicants disclose solely a capacitor coupled between the involved electrodes, such that one of ordinary skill would understand that the so called "solely via the capacitive coupling" is directed to solely a capacitor, or in the alternative, to a capacitor whose parasitic elements are so trivial as to be of no concern. Thus, regardless of which alternative is taken, an ideal capacitor or real world capacitor with imperfections, the capacitive coupling to the involved electrodes provides a potential at the charging FET gate electrode solely by the capacitive coupling as claimed.

Since this issue is being raised for the first time by the Answer, if further evidence is required of applicants directed to the conclusonary statements of the Answer, then applicants will be willing to comply with such a request. Applicants, however, believe that such further evidence is not required, as the Answer has not supplied the required evidence supporting a convincing line of reasoning that applicants specification does not support the claimed subject matter.

One of ordinary skill ordinarily does not consider such parasitic elements when referring to electronic components disclosed in patents, but rather deal with ideal components. Such ancillary matters as to imperfect components are dealt with by those of ordinary skill in practical real world situations, which are not the same as presenting disclosures in a patent teaching how to make and use. That is not a concern of typical patent disclosures.

Patent disclosures are directed toward those of ordinary skill. The raising of the issue of irrelevant parasitic or imperfect elements in regard to a patent disclosure of electronic components is hypertechnical and is not proper. One of ordinary skill would understand the claims directed to a capacitor that provides a potential at the gate electrode solely by the capacitive coupling is in fact being coupled by a either real world or ideal capacitor, it matters not which, as disclosed by applicants.

One of ordinary skill knows the difference. A real world capacitor as disclosed by applicants in their application can also be such an ideal capacitor and no evidence is provided by the Answer that the disclosed capacitor exhibits imperfections that would produce an effective ESR undesired potential at the gate electrode such as to deny supporting the claim in issue. Even if it did exhibit such ESR, such is still being

provided solely by the capacitive coupling and not be some other direct ohmic connection as expressly excluded as disclosed by the specification. One of ordinary skill would so make and choose such a capacitor to function as disclosed to achieve the desired result to solve the problem addressed.

See applicants' specification page 1, line 24 to page 3, line 7 as to a discussion of the problem. One of ordinary skill would understand from applicants' disclosure that the desired disclosed capacitor is constructed based on the disclosed principles to achieve the disclosed improvement and not be concerned with some hypertechnical problem raised by the answer.

The issue raised by the answer is improper and should be disregarded as not applicable to the instant case. Applicants have complied with the requirements of 35 USC 112, 1st paragraph, as normally would be done by one of ordinary skill and the statute does not require more. The Examiner should be reversed as to this issue and all claims allowed.

Respectfully submitted,
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